

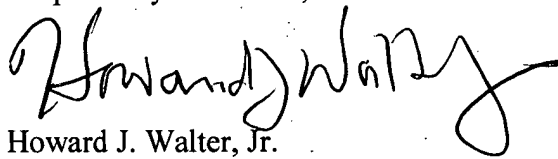
29. The method of co-planarizing copper or copper-based metallurgy and a refractory metal-based barrier layer or liner in an interlevel dielectric of a semiconductor device comprising the steps of:

planarizing said copper or copper-based metallurgy using a first slurry comprising an oxidizing agent comprising ferric nitrate, an oxidation inhibitor, a surfactant and an abrasive comprising alumina in water; said first slurry having a pH of between 1.2 and 2.5 and said first slurry capable of removing copper selectively with respect to said barrier layer or liner;

co-planarizing said barrier layer or liner and said interlevel dielectric using a second slurry comprising a peroxide agent, an oxidation inhibitor, a surfactant and an abrasive comprising silica in water; said second slurry having a pH of between 3.0 and 7.5 and said second slurry capable of removing said barrier layer or liner.

30. The method of claim 29 wherein said surfactant comprises a sulfated fatty acid.

Respectfully submitted,



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